

Figure 2 is a cross-sectional view of a semiconductor device 10. The device features a substrate 18 with a P+ region 28. An N-region 70 is formed in the substrate, with a width  $L_{\text{new}}$ . A dashed line 74 indicates the original N-region boundary, with a width  $L_{\text{Conventional}}$ . The N-region 70 is surrounded by a P+ region 68. A gate stack 60 is formed on top of the N-region, with a width  $L_{\text{new}}$ . The gate stack 60 includes a gate oxide 62, a gate dielectric 64, and a gate electrode 66. The gate electrode 66 is connected to a voltage source  $V_+$ . The gate oxide 62 is labeled 78, 80, 82, 84, 86, 88. The gate dielectric 64 is labeled 72, 56, 70. The gate electrode 66 is labeled 76, 94. The P+ region 68 is labeled 66, 76. The N-region 70 is labeled 72, 56, 70. The substrate 18 is labeled 18, 28. The P+ region 28 is labeled 28. The gate stack 60 is labeled 60. The gate oxide 62 is labeled 62. The gate dielectric 64 is labeled 64. The gate electrode 66 is labeled 66. The voltage source  $V_+$  is labeled  $V_+$ . The current  $I_H$  or  $I_L$  is indicated by an arrow pointing down.

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FIG. 3

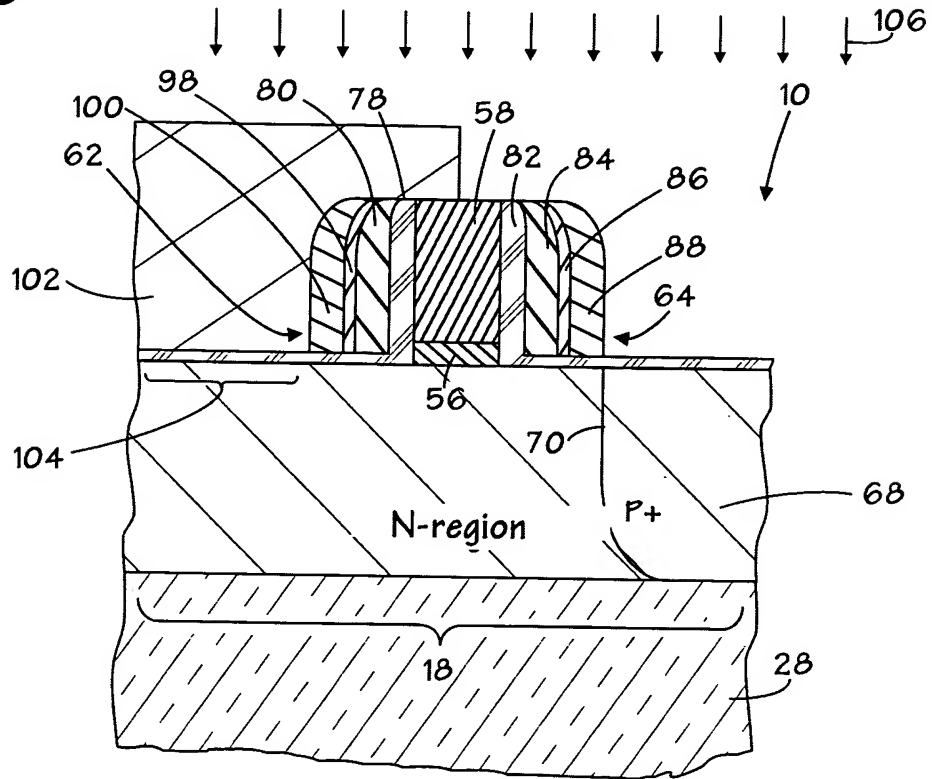
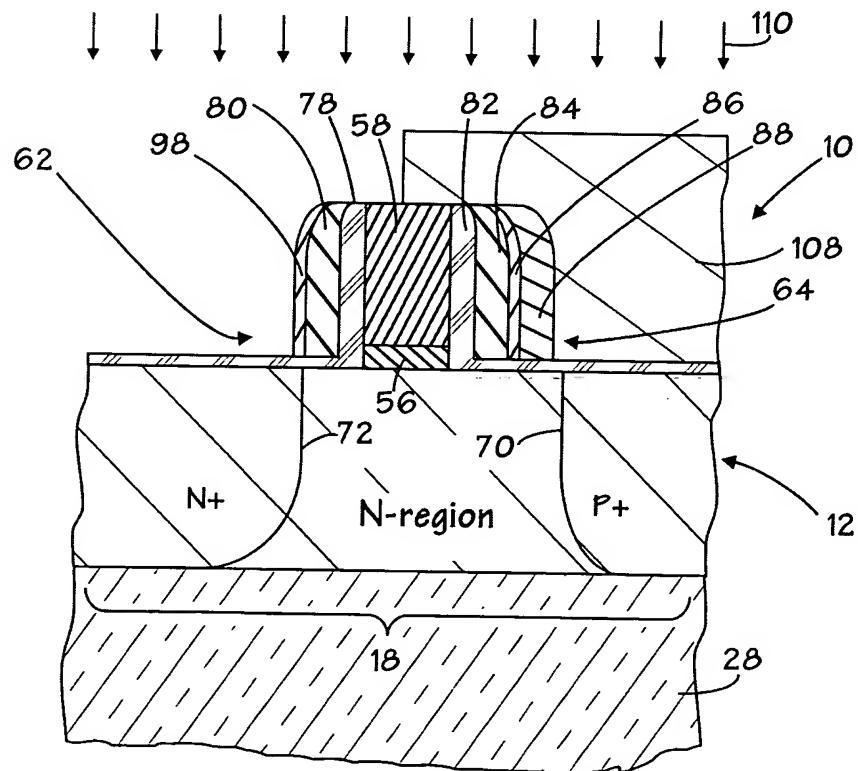


FIG. 4





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FIG. 5

